CLAIMS

What is claimed is:

1. A vertical tunneling transistor, comprising:

a channel disposed on a substrate;

a quantum dot disposed so that the channel is between the quantum dot and the substrate;

a gate disposed so that the quantum dot is between the gate and the channel; and

wherein an axis through the channel, the quantum dot, and the gate is substantially perpendicular to an upper surface of the substrate.

2. The vertical tunneling transistor set forth in claim 1, comprising a source disposed on the substrate adjacent to the channel.

3. The vertical tunneling transistor set forth in claim 1, comprising a drain disposed on the substrate adjacent to the channel.

4. The vertical tunneling transistor set forth in claim 1, comprising a tunneling barrier disposed between the channel and the quantum dot.

5. The vertical tunneling transistor set forth in claim 1, comprising an insulative layer disposed between the quantum dot and the gate.

6. An integrated circuit device, comprising:

a substrate; and

a memory array that includes a plurality of memory cells disposed on the substrate, each of the plurality of memory cells comprising a memory element and an access transistor, the access transistor comprising:

a channel disposed on the substrate;

a quantum dot disposed so that the channel is between the quantum dot and the substrate;

a gate disposed so that the quantum dot is between the gate and the channel; and

wherein an axis through the channel, the quantum dot, and the gate is substantially perpendicular to an upper surface of the substrate.

7. The integrated circuit device set forth in claim 6, comprising a source disposed on the substrate adjacent to the channel.

8. The integrated circuit device set forth in claim 6, comprising a drain disposed on the substrate adjacent to the channel.

9. The integrated circuit device set forth in claim 6, comprising a tunneling barrier disposed between the channel and the quantum dot.

10. The integrated circuit device set forth in claim 6, comprising an insulative layer disposed between the quantum dot and the gate.

11. An electronic device, comprising:

a processor adapted to execute instructions;

a storage device adapted to store data that comprises instructions to be executed by the processor;

a user input device adapted to receive data for use by the processor from a user;

a display device adapted to produce an image for viewing by a user based on instructions executed by the processor; and

a memory device that receives information stored on the storage device, the memory device comprising:

a substrate; and

a memory array that includes a plurality of memory cells disposed on the substrate, each of the plurality of memory cells comprising a memory element and an access transistor, the access transistor comprising:

a channel disposed on the substrate;

a quantum dot disposed so that the channel is between the quantum dot and the substrate;

a gate disposed so that the quantum dot is between the gate and the channel; and

wherein an axis through the channel, the quantum dot, and the gate is substantially perpendicular to an upper surface of the substrate.

12. The electronic device set forth in claim 11, comprising a source disposed on the substrate adjacent to the channel.

13. The electronic device set forth in claim 11, comprising a drain disposed on the substrate adjacent to the channel.

14. The electronic device set forth in claim 11, comprising a tunneling barrier disposed between the channel and the quantum dot.

15. The electronic device set forth in claim 11, comprising an insulative layer disposed between the quantum dot and the gate.

16. A method of producing a vertical tunneling transistor on a substrate, the method comprising the acts of:

disposing a channel on a substrate;

disposing a quantum dot so that an axis through the channel and the quantum dot is substantially perpendicular to the substrate; and

providing a gate so that an axis through the channel, the quantum dot and the gate is substantially perpendicular to the substrate.

17. The method of producing a vertical tunneling transistor set forth in claim 16, comprising employing atomic layer deposition to provide the channel.

18. The method of producing a vertical tunneling transistor set forth in claim 16, comprising employing atomic layer deposition to provide the quantum dot.

19. The method of producing a vertical tunneling transistor set forth in claim 16, comprising employing atomic layer deposition to provide the gate.

20. The method of producing a vertical tunneling transistor set forth in claim 16, comprising disposing a source adjacent to the channel.

21. The method of producing a vertical tunneling transistor set forth in claim 16, comprising disposing a drain adjacent to the channel.

22. The method of producing a vertical tunneling transistor set forth in claim 16, comprising providing a tunneling barrier.

23. The method of producing a vertical tunneling transistor set forth in claim 16, comprising employing atomic layer deposition to provide a tunneling barrier.

24. The method of producing a vertical tunneling transistor set forth in claim 16, comprising providing an insulative layer.

25. The method of producing a vertical tunneling transistor set forth in claim 16, comprising employing atomic layer deposition to provide an insulative layer.

26. A vertical tunneling transistor, the vertical tunneling transistor produced by the process of:

disposing a channel on a substrate;

disposing a quantum dot so that an axis through the channel and the quantum dot is substantially perpendicular to the substrate; and

providing a gate so that an axis through the channel, the quantum dot and the gate is substantially perpendicular to the substrate.

27. The vertical tunneling transistor set forth in claim 26, wherein the process comprises employing atomic layer deposition to provide the channel.

28. The vertical tunneling transistor set forth in claim 26, wherein the process comprises employing atomic layer deposition to provide the quantum dot.

29. The vertical tunneling transistor set forth in claim 26, wherein the process comprises employing atomic layer deposition to provide the gate.

30. The vertical tunneling transistor set forth in claim 26, wherein the process comprises disposing a source adjacent to the channel.

31. The vertical tunneling transistor set forth in claim 26, wherein the process comprises disposing a drain adjacent to the channel.

32. The vertical tunneling transistor set forth in claim 26, wherein the process comprises providing a tunneling barrier.

33. The vertical tunneling transistor set forth in claim 26, wherein the process comprises employing atomic layer deposition to provide a tunneling barrier.

34. The vertical tunneling transistor set forth in claim 26, wherein the process comprises providing an insulative layer.

35. The vertical tunneling transistor set forth in claim 26, wherein the process comprises employing atomic layer deposition to provide an insulative layer.